第33卷 第4期 发 光 学 报 Vol. 33 No. 4
2012年4月 CHINESE JOURNAL OF LUMINESCENCE Apr., 2012

Article ID: 1000-7032(2012)04-0428-05

Memory Effect and Charge-transport Mechanisms of Write-once-read-many-times Bistable Devices Based on ZnS Quantum Dots Embedded in Poly-4-vinyl-phenol Layer

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Abstract: A write-once-read-many-times (WORM) bistable device was prepared, in which ZnS quantum dots doped poly-4-vinyl-phenol (PVP) layer was sandwiched between ITO anode and Al cathode. Current-voltage (*I-V*) curves showed a switching characteristic with a large ON/OFF ratio of 10^4. The electrical bistability properties and charge-transport mechanisms were discussed in detail based on *I-V* characteristics. The conduction mechanisms in both ON- and OFF-states were discussed in terms of different theoretical models. The data-retention characteristics of the current-time (*I-t*) curve exhibited permanent retention ability at ambient conditions.

Key words: OBD; ZnS quantum dots; charge-transport mechanism; poly-4-vinyl-phenol
CLC number: O626 **Document code**: A **DOI**: 10.3788/fgxb20123304.0428

基于ZnS量子点与聚合物混合层的有机双稳态器件的记忆特性及其载流子传输机制

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摘要: 用ZnS量子点与poly-4-vinyl-phenol (PVP)复合,通过简单的旋涂法制备了结构为ITO/ZnS:PVP/Al的一次写入多次读取(WORM)的有机双稳态器件。器件起始状态为OFF态,通过正向电压的作用,器件由OFF态转变为ON态,并且在正向或反向电压的作用下,器件始终保持在ON态,表现出良好的一次写入多次读取的存储特性。与不含ZnS量子点的器件相比,含有ZnS量子点的器件表现出明显的双稳态特性,其电流开关比达到10^4,这说明ZnS量子点在器件中起到存储介质的作用。通过对器件电流-电压(*I-V*)特性的测试,详细

收稿日期: 2012-02-12; **修订日期**: 2012-02-22
基金项目: 国家自然科学基金(60877029,10904109,60977035,60907021); 天津自然科学基金(11JCYBJC00300,09JCYBJC01400)资助项目
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讨论了器件的双稳态特性以及载流子传输机制,并且用不同的传导理论模型分析了器件在 ON 态和 OFF 态的电流传导机制。器件 *I-t* 曲线表明器件在大气环境中具有良好的永久保持特性。

关 键 词: 有机双稳态器件; ZnS 量子点; 电荷传输机制; 聚乙烯基吡咯烷酮

1 Introduction

Solution-processed electrical bistable device based on hybrid inorganic/organic nanocomposite has emerged as a promising candidate for the next generation nonvolatile memory devices due to its low cost, low power consumption and high storage density[1-4]. Such hybrid devices containing inorganic nanoparticles (NPs) are being actively pursued and have been developed. Among the various memory devices, write-once-read-many-times (WORM) memory devices have become particularly interesting because of their extensive applications in rapid storage equipment[5]. Organic bistable devices (OBD) have been fabricated by simple solution process method, in which semiconductor nanocrystals such as CdSe[6], Cu_2S[7], ZnO[8], and CdSe/ZnS[9] were embedded into an organic matrix. However, high device performance has not yet emerged and the charge-transport mechanisms have been in heavy demand.

As a typical Ⅱ-Ⅵ compound semiconductor material, ZnS in nanoscale prepared via convenient routes was shown to be an effective luminescent material for lighting and display devices[10-13]. In this letter, we reported ZnS QDs WORM OBD for the first time. The OBD was fabricated utilizing the blends of ZnS QDs and PVP by spin-coating method. Current-voltage (*I-V*) measurements were performed to investigate the electrical bistability properties and the carrier transport mechanisms. Current-time (*I-t*) measurements were taken to investigate the permanent retention properties of the device.

2 Experiments

The cocktail of ZnS QDs and PVP was prepared by mixing ZnS QDs with PVP in a mass ratio of 2∶1 in methanol. The device was fabricated on an indium-tin-oxide (ITO)-coated glasses with a sheet resistance of 20 Ω/□. The ITO substrates were alternately cleaned ultrasonically in detergent, deionized water, acetone and isopropyl alcohol solutions, and subsequently dehydrated in vacuum at 100 ℃ for 30 min. Then the mixture was spin-coated onto the ITO substrate at 2 000 r/min for 20 s, and the film was baked at 100 ℃ for 15 min to remove residual solvent. Finally, on the top of the ZnS QDs and PVP composite layer, aluminum (~150 nm thick) was thermally evaporated as the top electrode. The schematic diagram of the final device is shown in Fig. 1. For reference measurement, the device without ZnS QDs was fabricated under the same condition. *I-V* and the *I-t* measurements were performed by Keithley 2400 Sourcemeter. All the electrical measurements of devices were carried out in ambient environment without any encapsulation.

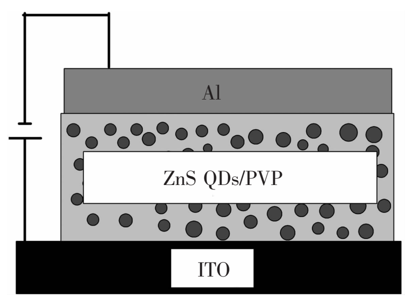

Fig. 1 Schematic diagram of the ITO/ZnS QDs embedded in PVP layer/Al device structure

3 Results and Discussion

Fig. 2 shows the *I-V* curves for the ITO/ZnS QDs embedded in PVP layer/Al and ITO/PVP/Al devices, measured with a closed loop voltage (0 ~ 5 ~ 0 ~ −5 ~ 0) V. An electrical hysteresis is clearly observed in the *I-V* curves for the ITO/ZnS QDs embedded in PVP layer/Al device, which displays different currents of a high-conducting state (ON-state) and a low-conducting state (OFF-state) at

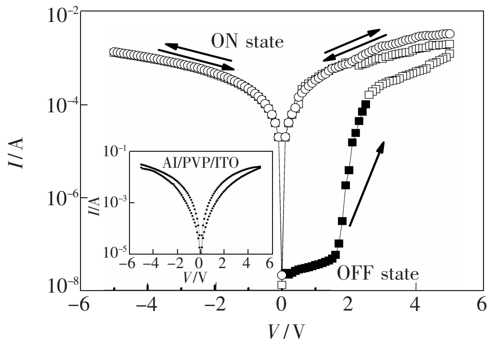

Fig. 2 Current-voltage curves with current expressed in logarithmic coordinates for the ITO/ZnS QDs embedded in PVP/Al device. The inset shows the *I-V* curves of the ITO/PVP/Al device

the same sweeping voltage. Comparing with the curve whose device without ZnS QDs (inset of Fig. 2), this large hysteresis shows an essential feature of the electrical bistable devices[3,14]. This indicates the crucial role of ZnS QDs in the OBDs. For the initial applied voltage from 0 to 5 V, the *I-V* curve for the ITO/ZnS QDs embedded in PVP/Al device, denoted by the filled rectangles, shows the OFF state. When the applied voltage is 1.8 V, the device current abruptly increases, which corresponds to a transition from the OFF-state to the ON-state. The transition from the OFF-state to the ON-state is regarded as the writing process for the WORM bistable device. After the device changes from the OFF-state to the ON-state, the ON-state current is maintained under either forward and reverse voltages between 5 and −5 V, as denoted by empty rectangles. The ON-state cannot back to the OFF-state under a reverse voltage smaller than −5 V or a forward voltage larger than 5 V, which indicates permanent memory retention in the WORM bistable devices. The maximum ON/OFF current ratio of the device containing ZnS QDs is approximately 1.16×10^4 at applied voltage of 1.5 V, and that of the device without ZnS QDs is about 2.8, indicating that the ZnS QDs act as stable data-storage media in PVP layer[15].

The memory retention ability of the device is very important for achieving high-performance devices in practical applications. The retention time of the ON- and OFF- states was measured under a constant bias voltage of 1.5 V, as shown in Fig. 3. The ON-state current was monitored by repeating the reading process after the writing process. The device remained in the ON-state for 10^4 s without any significant degradation, meaning the excellent environmental stability of the device.

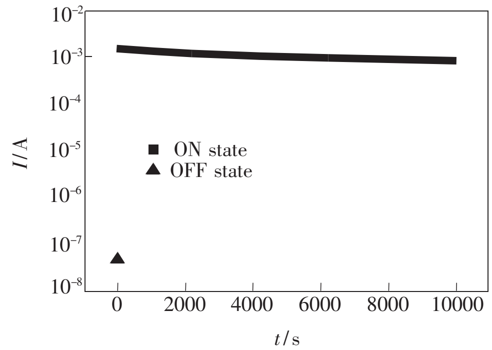

Fig. 3 Current retention characteristics of the ITO/ZnS QDs embedded in PVP/Al device under a constant voltage of 1.5 V

The data fitting of the *I-V* curves was performed to clarify the memory mechanisms and the charge-transport mechanisms. As shown in Fig. 4, the *I-V* curves in both states are fitted in terms of different theoretical models. For the OFF-state, the log(I)-log(V) plot can be divided into three regions (a) ~ (c) with distinctively different slopes. In the region (a), the *I-V* curve can be fitted to a straight line of 0.8 by employing the Ohmic model, which is expressed as

$$J = qn\mu V/d^{[16]}, \tag{1}$$

wherein, q is the number of charges per carrier, n is the density of charge carriers, μ is the mobility of charge carriers, and d is the thickness of the film.

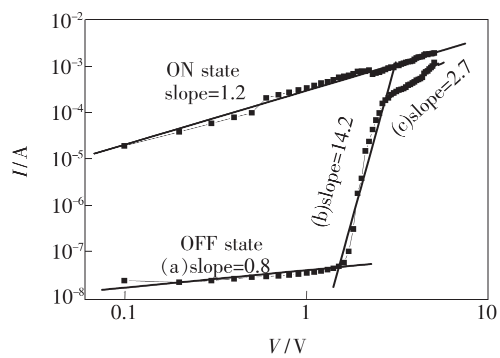

Fig. 4 The fitting results of the *I-V* characteristics of the ITO/ZnS QDs embedded in PVP layer/Al device on a double logarithmic scale in the ON state and in the OFF state

This suggests that Ohmic current is probably the main conduction at the low forward voltage.

In the region (b), a straight fitting line with a slope of 14.2 is obtained in the scanning voltage from 1.6 to 2.7 V, which was known as trap-controlled charge-limit-current(TCLC) model, suggesting the presence of traps distribute exponentially within the forbidden gap[17]. There exists a distribution of surface charge traps for ZnS QDs which have a dramatic influence on carrier behavior driven by applied electric field. ZnS QDs embedded in PVP layer are considered to act as charge traps and to produce significant hysteresis.

For curve in region (c), the data can be simulated by the space-charge limited model[18]

$$J = 9\varepsilon\varepsilon_0\mu V^2/8d^3, \quad (2)$$

in which, ε is the dielectric constant of the material and ε_0 is the permittivity of free space. The fitting plot yields a slope of 2.7, indicating that the current conduction is dominated by the space-charge limited current (SCLC) effects.

A straight line with a slope of 1.2 for ON-state in Fig. 4 suggests that the current is determined by the Ohmic conduction. Under a positive voltage applied, the electrons can be captured by ZnS QDs and the traps are nearly filled with voltage at 5 V, resulting in a reduction of the space charge effect. When the applied voltage decreased from 5 V, electrons injection can penetrate across the active layer of hybrid PVP-ZnS QDs.

4 Conclusion

In summary, we observed the electrical bistability properties and charge-transport mechanisms in WORM bistable devices based on ZnS QDs embedded in a PVP layer. The *I-V* curves of the ITO/ZnS QDs embedded in PVP layer/Al device show an apparent electrical hysteresis. The fitted data of the *I-V* curves for the device were used to explain the carrier behavior in the device, and the conduction mechanisms in both ON- and OFF-states were modeled by an Ohmic and space-charge limited current. The maximum ON/OFF current ratio of the WORM bistable device was as large as 10^4, and the data-retention characteristics of the *I-t* curve for the device exhibited permanent retention ability at ambient conditions. It provides a potential application of nanoparticles in next-nonvolatile WORM memories.

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